Amendments to the Claims

1. (currently amended) A network device, comprising:

a first port to allow the device to communicate with other devices on an expansion bus;

a second port to allow the device to communicate with devices on a ~~second~~ system bus;

a memory to store data; and

a processor to:

receive a set of data from an expansion device on the expansion bus in a data path;

receive an interrupt signal intended for a system processor from the expansion device on the expansion bus in a command path and to prevent the interrupt signal from reaching the system processor in the command path;

transmit the set of data into a transaction queue in a data path to the system processor;

generate an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor; and

insert the indicator into the transaction queue in the data path to a system memory associated with the system processor after the set of data;

generate a read request to the expansion device.

2. (original) The network device of claim 1, the network device further comprising a peripheral component interconnect bridge.

3. (canceled)

4. (currently amended) The network device of claim 1, ~~the second bus being~~ wherein the second port allows the device to communicate with devices on an expansion bus.

5. (original) The network device of claim 1, the processor to generate an indicator of completion further comprising the processor to generate a transaction addressed to a predetermined area of a system memory.

6. (canceled)

7. (currently amended) The network device of claim 6 1, the processor to insert the indicator further comprising the processor to transmit data from the read request to a predetermined address in a system memory.

8. (currently amended) A method, comprising:

receiving a set of data from an expansion device on an expansion bus in a data path;

receiving an interrupt signal intended for a system processor from the expansion device on an expansion bus in a command path indicating a data transfer is complete and preventing the interrupt signal from reaching a system processor;

inserting the set of data from the data transfer into a transaction queue of the data path to the system processor;

generating an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor; and

inserting the indicator into the transaction queue of the data path to a system memory associated with the system processor after the set of data;

generating a read request to the expansion device.

9. (original) The method of claim 8, generating an indicator of completion further comprising generating a transaction addressed to a predetermined area of a system memory.

10. (original) The method of claim 9, inserting the indicator further comprising inserting the transaction into the transaction queue.

11. (canceled)

12. (currently amended) The method of claim ~~11~~ 8, inserting the indicator into the transaction queue further comprising inserting data from the read request into the transaction queue, addressed to a predetermined area of a system memory.

13. (original) The method of claim 8, the method further comprising:

receiving data from network device;

receiving the indicator at a predetermined area of memory;

generating an interrupt to a system processor in response to the indicator; and

processing the data from the network device.

14. (currently amended) A network device, comprising:

a means for allowing the device to communicate with other devices on a first bus, the first bus being an expansion bus;

a means for allowing the device to communicate with devices on a second bus, the second bus being a system bus;

a means for storing data; and

a means for:

receiving a set of data from an expansion device on the expansion bus in a data path;

intercepting an interrupt signal intended for a system processor from the expansion device on the expansion bus in a command path and preventing the interrupt signal from progressing to the system processor;

inserting the set of data into a transaction queue in data path to the system processor;

generating an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor; and

inserting the indicator into the transaction queue in the data path to a system memory associated with the system processor after the set of data;

generating a read request to the expansion device.

15. (original) The network device of claim 1, the network device further comprising a peripheral component interconnect bridge.

16. (canceled)

17. (original) The network device of claim 1, the means for allowing the device to communicate with device on a second bus further comprising a means to allow the device to communicate on a second expansion bus.

18. (currently amended) An article of computer-readable media containing instructions that, when executed, cause the computer to:

receive an interrupt signal intended for a system processor from an expansion device on an expansion bus in a command path indicating a data transfer is complete and to prevent the interrupt signal from reaching a system processor;

insert a set of data from the data transfer received on a data path into a transaction queue in the data path;

generate an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor; and

insert the indicator into the transaction queue in the data path to a system memory associated with the system processor after the set of data; and

generate a read request to the expansion device.

19. (original) The article of claim 18, the instructions causing the computer to generate an indicator of completion further cause the computer to generate a transaction addressed to a predetermined area of a system memory.

20. (original) The article of claim 19, the instructions causing the computer to insert the indicator further causing the computer to insert the transaction into the transaction queue.

21. (canceled)

22. (currently amended) The article of claim ~~21~~ 18, the instructions causing the computer to insert the indicator into the transaction queue further causing the computer to insert data from the read request into the transaction queue, addressed to a predetermined area of a system memory.